REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Final Examiner's Action electronically delivered July 31, 2009. The Applicant respectfully requests reconsideration of this application in view of the following remarks.

The Applicants originally submitted Claims 1-20 in the application. In previous responses, the Applicant canceled Claims 5, 12 and 19 without prejudice or disclaimer. In the present amendment, the Applicants have amended Claims 1, 8, and 15. Support for the amendment can be found, *e.g.*, in paragraphs [0002], [0006], [0014], [0023], and [0030], and Fig. 2 of the original specification. Accordingly, Claims 1-4, 6-11, 13-18 and 20 are currently pending in the application.

I. Rejection of Claims 1-4, 6, 8-11, 13, and 15-18 under 35 U.S.C. §103

Previously, the Examiner rejected Claims 1-4, 6, 8-11, 13, and 15-18 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,689,516 to Mack, *et al.* (hereinafter "Mack") and further in view of U.S. Patent No. 5,515,523 to Kalkunte, *et al.* (hereinafter "Kalkunte") and U.S. Patent No. 7,124,340 to Bos, *et al.* (hereinafter "Bos"). The Applicant believes the invention as presently claimed, however, is neither shown nor suggested in the cited portions of the cited combination of Mack, Kalkunte, and Bos. More specifically, the Applicant fails to find where the cited portions of the cited combination of Mack, Kalkunte, and Bos, as applied by the Examiner, teaches or suggests denying access to a memory on an integrated circuit (IC) when a testing port is disabled as recited in now amended independent Claims 1, 8, and 15.

At the middle of page 2 of the Final Rejection of July 31, 2009, the Examiner states:

> "Mack teaches for use with an integrated circuit (IC) ...port access circuitry, coupled to said testing port, that enables said testing port based on said configuration (FIG.1, col. 3, lines 25-40, col. 6, lines 5-18 and lines 55-65, col. 7, lines 10-25)."

The cited portions of Mack teach that when a JTAG-disable cell, J_{DIS}, is programmed by a manufacturer of PLD 100 a logic one is provided on JTAG-reset line JTAG_RST which disables JTAG test circuitry 190 without affecting the functionality of the remaining circuitry of PLD 100. (*See, e.g.*, lines 9-16 of Mack.) Thus, the cited portions of Mack teach that when JTAG test circuitry on a PLD is found to be defective, a bit can be set by the manufacturer of the PLD to allow the rest of the PLD, *i.e.*, function block 302 which includes flash memory 310 and RAM 330, to function.

Claims 1, 8, and 15 have been amended, as noted above, to more clearly point out that when JTAG test circuitry on an IC is disabled, access to a memory in the IC is denied. As discussed above, Mack teaches that when JTAG test circuitry on a IC is disabled, access to the memory is allowed to occur as a normal operation of the PLD. As such, Mack does not teach the newly added limitation of denying access to a memory of an IC when a testing port is disabled. Furthermore, Mack does not suggest the same.

Mack is relates to separately testable JTAG circuitry and a mechanism for disabling defective JTAG circuitry without affecting the functionality of the remaining PLD circuitry where a user can access memory portions of the PLD, allowing manufacturers to make use of PLDs that otherwise would have been discarded as defective. (*See, e.g.*, col. 1, lines 19-30 and col. 2, lines 7-9 and 28-30 of Mack.) The invention as presently claimed is directed to disabling non-defective JTAG circuitry and not allowing access to memory portions of the IC. As such, Mack does not teach or suggest denying access to a memory on an IC when a testing port is disabled as recited in presently amended independent Claims 1, 8, and 15.

Kalkunte and Bos have not been cited to cure the above-noted deficiencies of Mack but to teach the limitations of partially disabling a port inhibit circuitry and allowing a direct loopback between input and output pins of a testing port. (*See* Final Rejection of July 31, 2009, pages 2-3.) As such, the cited portion of Mack in combination with the cited portions of Kalkunte and Bos, as applied by the Examiner does not provide a *prima facie* case of obviousness of presently amended independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 1-4, 6, 8-11, 13, and 15-18 and allow issuance thereof.

II. Rejection of Claims 7, 14, and 20 under 35 U.S.C. §103

Previously, the Examiner rejected Claims 7, 14, and 20 under 35 U.S.C. §103(a) as being unpatentable over Mack and further in view of Kalkunte, Bos, and U.S. Patent No. 6,522,100 to Hansford (hereinafter "Hansford"). As established above, the cited combination of the cited portions of Mack, Kalkunte, and Bos does not provide a *prima facie* case of obviousness of presently amended independent Claims 1, 8, and 15. Hansford has not been cited to cure the above-noted deficiencies of the cited combination but to teach wherein the IC is a baseband chip of a mobile communication device. (*See* Final Rejection of July 31, 2009, page 5.) As such, the cited combination of the cited portions of Mack, Kalkunte, Bos, and Hansford does not establish a *prima facie* case of obviousness of presently amended independent Claims 1, 8, and 15 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 7, 14, and 20 and allow issuance thereof.

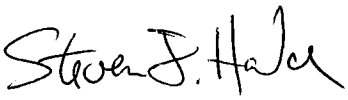
III. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-4, 6-11, 13-18, and 20.

The Applicant requests the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC



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